

**Lesson 3.1 Key Terms Sequential Logic Design**

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| Term | **Definition** |
| Asynchronous Counter | Type of counter in which each flip-flop output serves as the clock input signal for the next flip-flop in the chain.  |
| Asynchronous Inputs | Flip-flop inputs that can affect the operation of the flip-flop independent of the synchronous and clock inputs.  |
| Clock | Digital signal in the form of a rectangular pulse train or a square wave.  |
| Clocked D Flip-Flop | Type of flip-flop in which the D (data) input is the synchronous input.  |
| Clocked J-K Flip-Flop | Type of flip-flop in which inputs J and K are the synchronous inputs.  |
| D Latch | Circuit that contains a NAND gate latch and two steering NAND gates.  |
| Duty Cycle (DC) | Fraction of the total period that a digital waveform is in the HIGH state. DC = th/T (often expressed as a percentage: %DC = th/Tx100%).  |
| Edge-Sensitive | Manner in which a flip-flop is activated by a signal transition. A flip-flop may be either a positive- or a negative-edge-triggered flip-flop.  |
| Falling Edge | The part of a pulse where the logic level is in transition from a HIGH to a LOW.  |
| Flip-Flop | A sequential circuit based on a latch whose output changes when its CLOCK input receives a pulse.  |
| Frequency | The number of cycles per unit time of a periodic waveform.  |
| Level-Sensitive | Enabled by a logic HIGH or LOW level.  |
| Period | The amount of time required for one complete cycle of a periodic event or waveform.  |
| PRESET | Asynchronous input used to set Q=1 immediately.  |
| Propagation Delays (tPLH/tPHL) | Delay from the time a signal is applied to the time when the output makes its change.  |
| RESET / CLEAR | Asynchronous input used to set Q=0 immediately.  |
| Rising Edge | The part of a pulse where the logic level is in transition from a LOW to a HIGH.  |
| Sequential Logic | Digital circuitry in which the output state of the circuit depends not only on the states of the inputs, but also on the sequence in which they reached their present states.  |
| Shift Register | Digital circuit that accepts binary data from some input source and then shifts these data through a chain of flip-flops one bit at a time.  |
| State Machines | A sequential circuit that advances through several defined states.  |
| Synchronous Counter | Counter in which all of the flip-flops are clocked simultaneously.  |
| Trigger | Input signal to a flip-flop or one-shot that causes the output to change states depending on the conditions of the control signals.  |